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Review on Design and Analysis of ADC

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Abstract: Analog to Digital convertor is a mixed circuit with different signals taken as input. The analog signals such as voltages to digital 1's and 0's. In ADC's. There are two important features which are used to find out the conversion accuracy to represent the digital signals. The two factors which are important to find the accuracy of the data conversions is static and dynamic characters of ADC. In ADC, the type of measuring the signals varies with respect to the bit rate and sampling rate. The applications of ADC are measurement and control systems, industrial instrumentation, communication systems and all other sensor based systems. This paper analyzes the performance, resolution, sampling rate and power consumption of various types of an ADC.This paper reviews the performance of different types of ADC's such as flash , pipelined, successive approximation register type, dual slope and delta-sigma type ADC's.

Keywords: ADC, Resolution, sampling rate, Non-Linearity, Static parameters, Dynamic Parameters

1. Introduction

Analog to digital converter (ADC) is in analog and mixed-signal circuit which is used the most frequently for converting an analog input signal into digital output code word in microprocessors, microcontrollers, digital signal processing, speech and video processing architectures, communication devices and consumer electronics applications. It is a strap between analog and digital processing techniques to process the real-world analog signal and to produce the equivalent digital outputs for fast and accurate processing. Microprocessor performs only complex signal processing. When signals are in digitized form, they are less susceptible to adverse effects of additive noise. Analog to digital conversion is a two-step process.1) Quantizing i.e., dividing analog signal range to a set of discrete values.2) Encoding i.e., assigning a digital word to each state and matched to input signal.

This paper provides the resolution, offset error, gain error, accuracy and linearity of various analog to digital converters. The resolution defines the analog levels in number to develop respective digital output word. Each digital output code represent the equivalent analog voltage levels. Thus an N-bit data converter implies to resolve 2 to the power of N distinct analog levels. The Offset error is defined to be the digital output that has been generated for the analog input at starting position of the data conversion which is first position of data conversion. The gain error is defined to be digital the output that has been generated for the analog input at ending position of the data conversion which is last position of data conversion. The absolute accuracy of the data converter is defined as a difference of ideal and actual data transfer response of the converter. The term relative accuracy is denoted to as maximum value of the integral non linearity (INL) error. The converter may get less resolution than the actual resolution when the INL value have maximum variation. The precise level of conversion is measured by measuring the accuracy of converter which may be greater than the actual resolution defined in sampling. In order to measure the INL error, both offset and gain errors have to be removed before starting the measurement. The INL error is defined as the maximum deviation of the ADC from the ideal straight line. A conservative measurement of INL and DNL (differential non-linearity) uses the end points of the converter switching response from the ideal straight line. Typically, INL is calculated by slowly sweeping the ADCs analog input in its full-scale range.

2. The Design Structure of Various ADC's

Each ADC has its own trade-off. The sigma delta ADC have a great resolution whereas there is limited conversion speed. Consider the flash ADC which is fastest as the resolution increases, it becomes almost impossible to implement flash ADC beyond 8 to 10 bits. Pipelined ADC reduces the conversion time but suffers from high latency. Time interleaved ADC's are used for high speed applications. On the other hand SAR ADC gives a nice trade off where it requires N cycles for N bits.

3. Different Types of ADC's

3.1. A. Flash ADC

This is also known as parallel ADC which converts analog voltage to digital bits. The flash ADC is used in large bandwidth applications. Power consumption is high compared to other architectures. However this is highly expensive. The major components are comparators are voltage comparator and encoder. The number of comparators for 3 bit ADC is 8.If it is 4 bit ADC, 16 comparators are required. The disadvantage is high resolution so that more number of comparators leads to large area. The analog ramp or sine wave input voltage is applied to the analog comparator to compare the analog input voltage levels with the reference input voltage. The parallel processing of comparison in the comparator is usually faster than other type of ADC structure in the comparison. And the parallel processing provide high data conversion speed to the converter. Separate sample and hold circuit is not needed to this flash ADC.

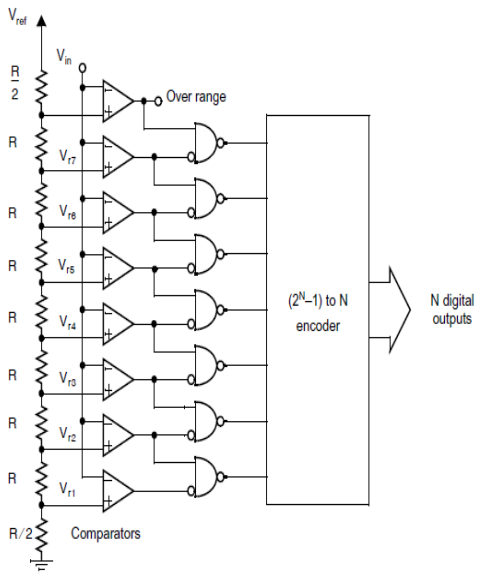


Fig.1. Block diagram of the flash type ADC

The resistive ladder circuit connected before the analog comparators provide reference voltage to the comparison process. The reference voltages are generated from the reference magnitude by voltage divider rule. In the comparators, trans conductance type comparative circuit is used to compare and amplify the differences of the analog input voltage and the reference input voltage. The thermometer code generated by the parallel comparator is applied to the encoder to convert thermometer code into digital binary output code.

3.2. Pipelined ADC

This architecture of pipeline is more popular for the signals ranging for 1Msps to 100Msps. The frequent usage of pipeline systems performs signal operation in ever stage and produces output for the following sampler. As the output would be generated then the same operation is performed for the following samplers. Pipelined architectures are efficient if several of operations are combined. The area and the power dissipation grows linearly with the number of bits. The gain is necessary between the stages to avoid data corruption. The wide range of applications as CCD imaging, ultrasound medical imaging, cable modems and fast ethernets are done using these sampling rate and resolutions.

The first sample of the signal is sampled and is kept as hold until the next sample. And in flash ADC the same is quantized into 3bits. This generated signal is given to 3 bit digital to analog converter so that output in analog form gets deducted from the given signal. This signal is fed to next stage with an increased residue factor of 4.

As the Flash ADC requires 4 least significant bits , the pipeline ADC continues to provide 3 bits from the overall residue. All the bits which are same as the sample are combined with respect to the shift registers which are then fed to digital logic to rectify the errors and the bits are redefined with different points of time. This process continues for the next generated sample. The reason for the high output generation is pipeline ADC.

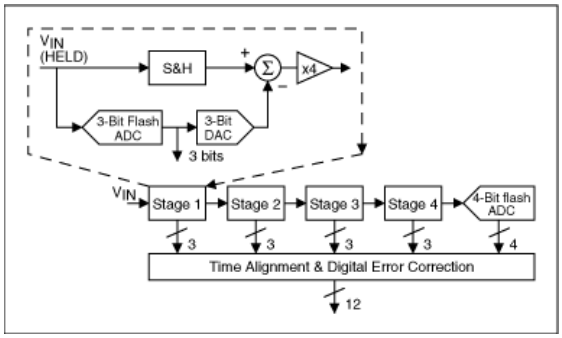


Fig.2. Block diagram of the pipelined ADC

3.3. Successive Approximation ADC

The amazing versatility is the main reason for this type of ADC i.e, Successive Approximation technique to be popular. The conversion time is

very fast and also provide very high accuracy rate. This type of ADC can operate in both high and low power cases. These ADC's requires simple circuits to generate the signals which have only one comparator, and a bunch of capacitors with some switched to operate the logic of digital signals.

Consider the game of guessing a number from 1 to 128 where the answer will be a yes/no randomly. If the number is greater than 64 and then if yes, verify if the number is greater than 96 or not. Or if the number is not greater than 64 then verify the number is more than 32. Then the final question divides the search into two different steps and the operation again continues to generate the estimated output.

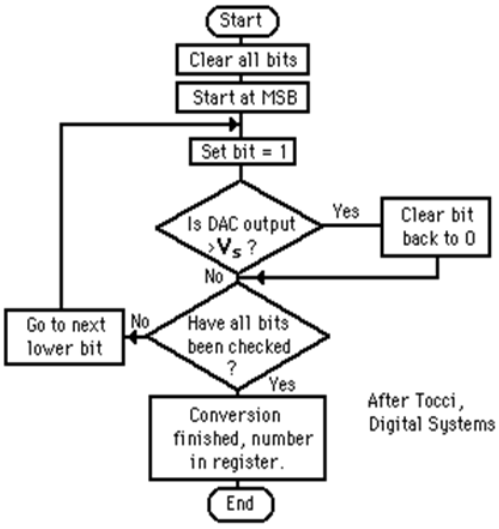


Fig.3. *Block diagram of the Successive Approximation ADC*

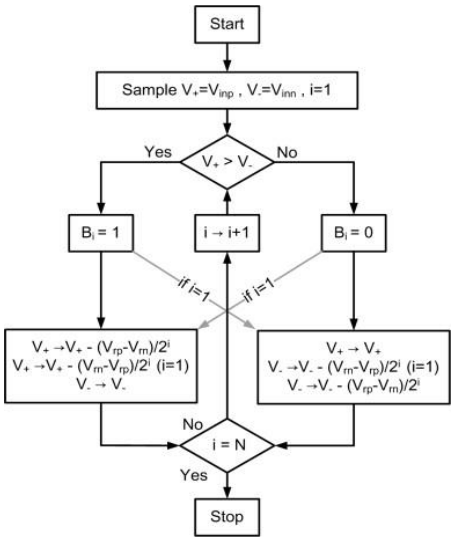


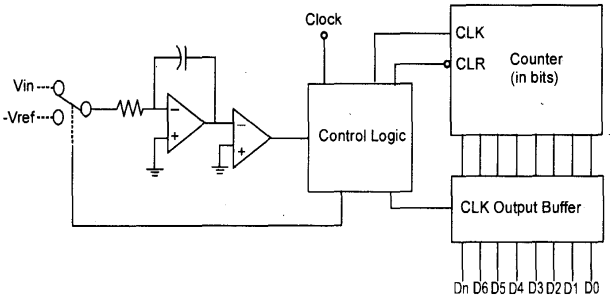
Fig.4. *Binary Selection procedure of Successive Approximation ADC*

3.4. Dual slope ADC

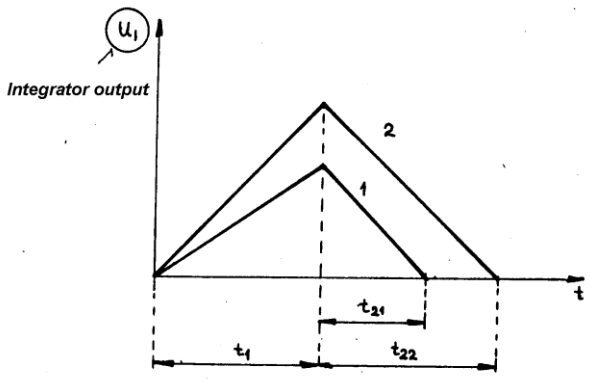
The fundamental components of dual slope ADC are integrator circuit, electronically controllable switches, data counter, clock signal generator, control logic circuit and analog voltage comparator. The conversion result is insensitive to errors in component values. Fewer adverse effects from noise. The accuracy is higher which depends on use of precision external components.

The output depends on analog input voltage but not on time constant or resistor or capacitor. A Dual slope ADC integrates an unknown input voltage for a fixed amount of time then disintegrates using a known reference voltage for variable amount of time.

The key advantage of this architecture over single slope is that final conversion result is insensitive to errors in component values that is any error introduced by the component value during integrate cycle will be cancelled out during disintegrate phase.



(a)



(b)

Fig.5. *(a) Block diagram of the dual slope ADC (b) Dual slope conversion time slot in conversion*

At phase-1 the time is fixed and the slope is variable. At phase-2 the time is variable and slope is fixed. At time<0, s1 is set to ground, s2 is closed and counter becomes zero. At time=0, the conversion begins and s2 is open and s1 is set so input to integrator is input voltage. S1 is held for time interval which is a constant predetermined time interval. When s1 is set the counter begins to count clock pulses the counter resets to zero after time interval. The output voltage of integrator at time interval is linearly proportional to input voltage. At time interval s1 is set so reference voltage is input to the integrator which has a voltage stored in it. The integrator voltage then drops linearly with a slope –Vref/RC. A comparator is used to determine when the output voltage of integrator crosses zero. When it is zero, the output value is a state of the counter.

3.5. Dual slope ADC

Delta Sigma (ΔΣ) is the fastest and modern ADC with advanced features. In this type of ADC, the integrator and the analog signal are connected to produce a rate changing voltage called slope with respect to magnitude as output. The comparator compares the ramping voltage and the ground stage potential and produces a one bit output to the ADC which is either high or low which depends upon the integrator output which may be positive or negative, this is then connected to D-flipflop clocked with a very high frequency. This is again fed back to the integrator which directs to 0 voltage. The summing integrator is in the left part of the circuit. The comparator also works as 1-bit ADC. The next input to the summing integrator is comparator. The D type flipflop then generates the output either high or low to the comparator and produces this result to the top of the circuit. The single polarity 0V/5V gets converted into +V/-V by using the last 1-bit ADC(comparator).

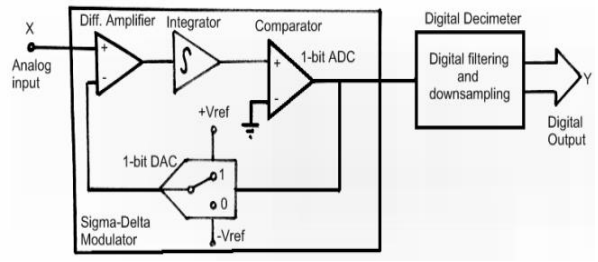


Fig.6. *Block diagram of the sigma delta ADC*

If the output is positive of the integrator then the signal “high” is produced in the comparator which is then connected to the D flip-flop. The last comparator which is a non-inverting input will follow the output “high” signal of the comparator to the Q-line for the next cycle of clock. This comparator detects if the in-out is greater than the threshold 1/2 +V, is in a positive direction , then it generated full +V signal to the input of the other integrator. The negative direction in the integrator is driven by the positive feedback signal. The feedback signal loops send a signal (-V) to the top of the integrator to make the output of the integrator positive if ever it becomes negative. So, the process of this sigma delta ADC is: first the difference between the integrator and the ground potential is recognized by the comparator (Δ) and secondly, the summing operation which is performed between the analog input and integrator (Σ).

This procedure lists the continuity of the bits output by the flip flop. If zero volts is generated by the analog then the integrator has no options to produce a output in either ways positive or negative except when there is a feedback signal is connected to it. At this moment, the output generated by the flipflop will continuously flip between “high” or “low”, to this the feedback signal continues its operation to keep the integrator at zero volts. Oversampling is a common effect on this type of ADC which occurs the difference between the operations performed. The concept where multiple samples of the input analog signal has been considered by the ADC which are then converted to the average of digital bits, in this case a 1-bit ADC. The number of bits are resolved which increases the affectivity of the result. At slower rate, the same process can be implemented by 8-bit ADC but with a slower rate of operation when compared with this 1-bit ADC with the operation of oversampling.

5. Conclusion

An ADC has multiple bits for best resolution, fast sampling rate, and fast generated outputs. Usually, it doesn’t actually work in the real world. Any of these qualities can be increased with additional circuit complexity and components. The higher the clock speed, the higher the resolution. The summary of all the different types of ADC are ranked for worst to best in the following:

Resolution: Flash ADC, Successive Approximation ADC, Pipelining ADC, Sigma Delta ADC, Dual-slope ADC.

Speed: Flash ADC, Successive Approximation ADC, Pipelining ADC, Sigma Delta ADC, Dual-slope ADC.

Power Consumption: Flash, Pipeline, Successive Approximation, Dual-slope, and Sigma-Delta.

All the ADC's mentioned are ranked w.r.t other factors also. For references, the step recovery of ADC's. A Dual slope ADC is the slowest and this follows with Successive Approximation ADC which are almost as equally fast with the input signal which totally depends upon the input analog signal.

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