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Linear Ramp Generator for ADC BIST

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Abstract: This paper presents a design of linear ramp generator for on-chip testing of analog to digital converter. Linear ramp signal is generated by the design of MOS transistor logic based ramp generator and applied to the converter for extending the test accuracy. The primary non-idealities affecting the linearity and timing of the ramp generator are discussed and overcome in this work. A comparator based feedback configuration is used to maintain the linearity and eliminate the offset in ramp voltage position and transient time, which are insistent requirements in on-chip analog and mixed-signal IC testing. The proposed linear ramp generator is implemented in 0.18µm CMOS technology, and the simulation results are observed to exhibit the performance and feasibility in analog to digital converter testing. The observed results show that the proposed ramp generator achieves oscillation frequency of 5 MHz with the power consumption of 113.74µW from 2V supply voltage. The effective layout area of ramp generator is 45.9µm*18.9µm.

Keywords: Integer order controllers, Fractional order controller, Level process, Blood glucose regulation, Biochemical reactor

1. Introduction

The fast growing technology in electronic circuit design allows integrating analog and digital circuit together on the same chip for high-quality analog and mixed-signal (AMS) applications. In recent years, the mixed signal system-on-chips (SoC) are playing a wide role in replacing the use of analog and digital devices separately in an integrated circuit. The deep sub-micron technology and a higher level of components integration demand the mixed signal SoC to continue the device for adding more functionalities, futures on the same chip with low power consumption, reduced cost, and high reliability. Meanwhile, the mixed signal circuit testing is becoming a dominant factor where a design of AMS device is overriding the technology in the design and development area [1, 5]. Different functional blocks present in the mixed signal SoC requires several test strategies for on-chip testing. The conventional AMS circuit test consists of a parameter specific test circuit for the analog block, and automatic test pattern generator (ATPG) and scan circuits for testing digital function. However, this test procedure will make a testing of an AMS circuit as more complicated with extended test time. Also in test cost estimation, this traditional testing method bump-up the chip cost with both front-end and back-end costs. Different kinds of testing methods are available for satisfactory test performance. The most common way of testing AMS circuit is DSP-based mixed signal testers which give high test quality, but claims test cost immensely. Also due to the restriction in accessibility and observability of nodes through input/output pins, this method faces the difficulties to maintain signal integrity and that reduce the accuracy.

Built-in self-test (BIST) is a possible solution for signal integrity since it offers an on-chip stimulus and output response analysis for testing multi-functional circuits. Ramp generator is a popular circuit used in on-chip analog to digital converter (ADC) circuit testing, in which the linearity of the generated signal dominates the accuracy of data transition [2]. Also, the use of on-chip ramp generator must satisfy the testing requirements in area overhead, test time, observability and controllability [3] with constant oscillation frequency [4]. This paper presents a linear ramp generator for ADC BIST. As the use of fewer transistor counts in proposed ramp generator, it is the best option for the time domain based on-chip ADC test. The digital conversion is verified in the TIQ comparator [1] with time variation. The linear ramp signal generated by the feedback configured ramp generator encounters the significant and difficult problems present in the data conversion.

2. Linear ramp generator

The proposed feedback configured linear ramp generator is shown in Fig.1. The circuit is constructed with a current source to charge the capacitor, a ground connected MOS transistor to discharge with reset (rst) control, and a comparator based feedback configuration for linear ramp generation. The negative feedback driven comparator acts as a current source.

It eliminates the offset in the output and delivers constant current for successive ramp generation. The transistors P1, P2, P4 and P5 act as a current mirror circuit. The transistors P4 and P5 are modelled to provide a constant current through biasing transistor P8. An inverter in the output section provides fast switching to obtain a linear ramp signal generation. The rst controlled pull-up transistor charges the capacitor linearly to the peak level when reset is zero. When rst is one, the pull-down in the inverter drains the charge of capacitor completely to zero and the pull-up block the path to the capacitor from the current source, which reduces the total power dissipation of the circuit. The resulting ramp voltage across the output is directly proportional to ramp time.

$$V_{ramp}(t) = \frac{I_C}{C}.T = \frac{\mu C_{ox}(W/L)}{C}.(V_{comp} - V_{th})^2.T \qquad (1)$$

Where, IC biasing current, T tramp time period, μ mobility of transistor, Cox gate oxide capacitance, W width, L length, C capacitance, Vth, threshold voltage, Vcomp is comparator output voltage ie., [2R1/(R1+R2)].Vramp. The total ramp time is

$$T = C.(V_H - V_L)(\frac{1}{I_{ch}} + \frac{1}{I_{dch}}) \approx \frac{1}{I_{ch}} C.(V_H - V_L) \qquad (2)$$

Where, Ich charging current, Idch discharging current, VH and VL the maximum and minimum peak of the ramp signal.

The capacitor is charged with constant current Ich for 98% of time toward the peak voltage and discharges with Idch (Idch=49Ich) for 2% of time towards lower limit and then the new cycle will begin. This limits the slew rate in the output of ramp generator for linear ramp generation.

The generated linear ramp signal is applied to the TIQ-Comparator based ADC proposed in [1]. The effectiveness of data conversion in the ADC can be verified from the time domain response of TIQ comparator. The linear ramp signal drives the comparator accurately with defined time period. A 4-bit fast switching linear TIQ comparator is used here to verify the data conversion in the time domain. The accurate time interval in the output switching shows the perfectness of data conversion. Time-based switching maintains linearity in ADC transitions. The switching voltage of TIQ comparator is expressed as

$$V_{switching} = \frac{\sqrt{\mu_p W_p / \mu_n W_n}.[V_{dd} - V_{tp}] + V_{tn}}{1 + \sqrt{\mu_p W_p / \mu_n W_n}} \qquad (3)$$

Where, μn and μp mobility of pull-down and pull-up transistor, Wn and Wp width of pull-down and pull-up transistor, Vtn and Vtp threshold of pull-down and pull-up transistor, Vdd supply voltage.

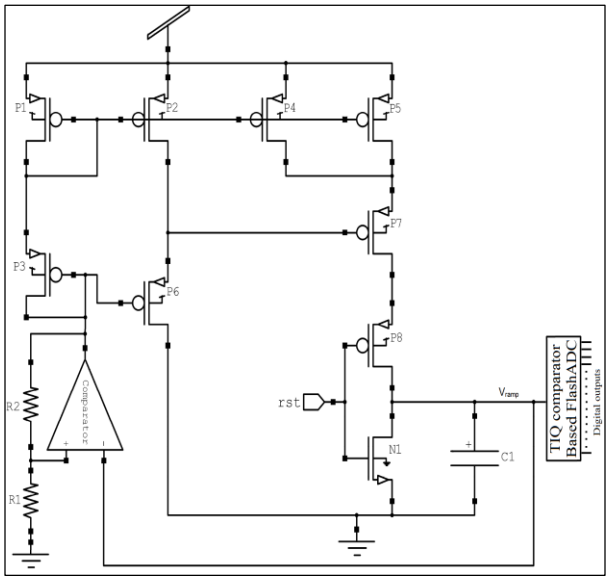

Fig.1 Proposed Linear Ramp generator for ADC testing

3. Result Analysis

The linear ramp generator has implemented in 0.18μm CMOS technology. Fig.2 shows the ramp signal generated by the proposed linear ramp generator with the oscillation frequency of 5 MHz from a supply voltage of 2V. Table.1 shows the spice simulation results for power dissipation, peak ramp voltage and duty cycle with different temperature values. The time domain based output observation in the TIQ comparator is shown in Fig.3, in which the comparators are designed with different W/L ratio as shown in Table.2 for accurate date conversion. The switching activity of comparator shows the effective data transition of ADC for the response of linear ramp input signal. The layout of linear ramp generator with TIQ comparator based ADC BIST is shown in Fig.4, in which the proposed ramp generator consume very less area when compared to ADC system. The active chip area of a ramp generator is 45.9μm × 18.9μm.

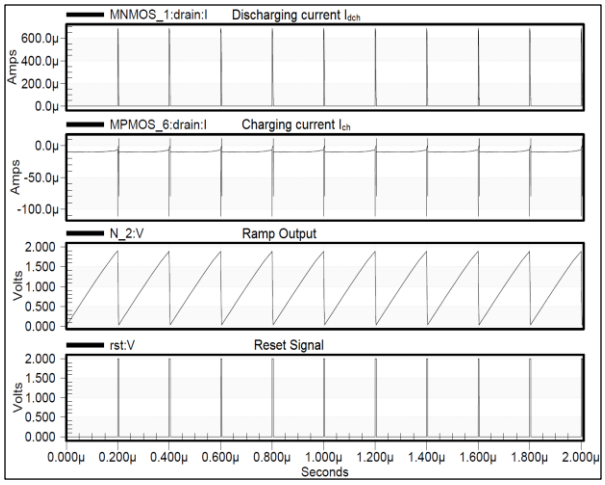

Fig.2 Simulation output of linear ramp generator

Table 1: Simulation results of linear ramp generator

Vcc	Technology	Temperature (°C)	Power Dissipation (µW)	Peak voltage of Ramp (in Volts)	Duty Cycle in (%)
2V	0.18µm	25	113.74	1.92	52.1
2V	0.18µm	30	113.28	1.89	51.8
2V	0.18µm	35	112.59	1.87	51.4
2V	0.18µm	40	112.00	1.84	51.1
2V	0.18µm	50	110.90	1.78	50.7

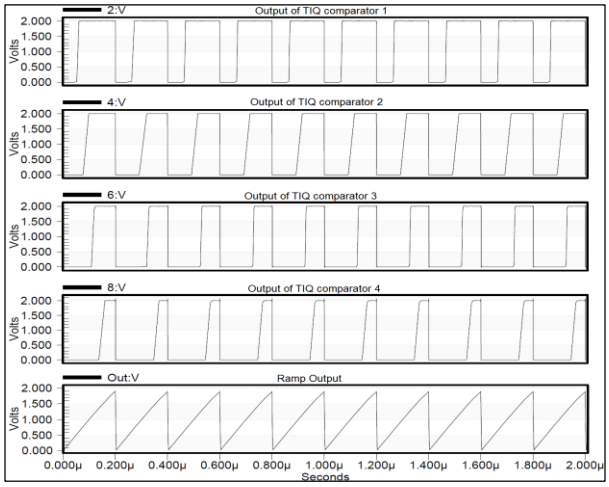

Fig.3 Output response of TIQ comparator for a linear ramp input

Table 2: Scaling of TIQ comparator

TIP Comparator	1	2	3	4
Channel Width in (µm)	1.5	1.5	1.5	1.5
Channel Length in (µm)	0.35	0.75	1.5	3.1

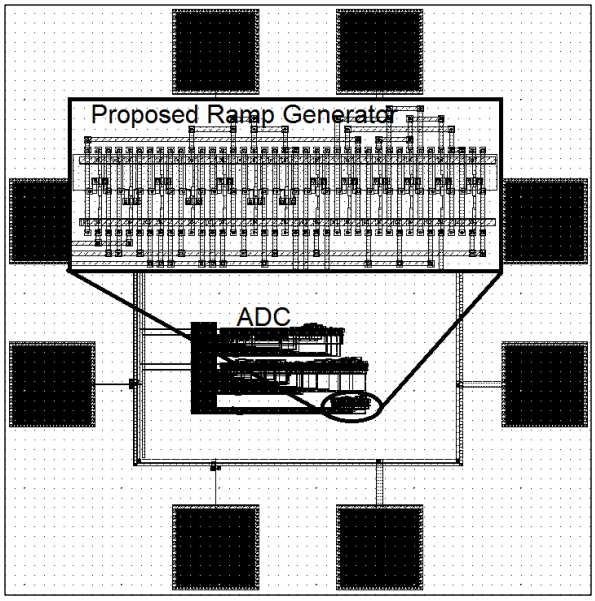

Fig.4. Layout design of proposed ramp generator

Conclusion: The linear ramp generator is proposed with TIQ comparator for ADC test. The output of TIQ comparator has verified for the effective data transition of ADC for the response of applied linear ramp input signal. The use of less transistor count in ramp generator has reduced the power and area of the test circuit. The linear ramp generator has integrated with TIQ comparators to observe the switching activity in ADC output. The test results show that the linear ramp input providing the accurate time in switching of ADC. Also, it results that the proposed linear ramp generator is efficiently switching the comparators of ADC for testing the functionalities.

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